SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-178459; filed on September 10, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

There is a vertical metal oxide semiconductor field effect transistor (MOSFET) in which a p type (or n type) semiconductor layer is buried in an n type (or p type) semiconductor layer, and which has a super junction structure (hereinafter, also referred to as a “SJ structure”) having an n type region and a p type region that are alternately arranged, as a semiconductor device for power control with a high breakdown voltage and a low ON resistance. In the SJ structure, the amount of n type impurities included in the n type region is equal to the amount of p type impurities included in the p type region, and thereby a non-doped region is simulatively formed and a high breakdown voltage is achieved. At the same time, a current flows through a region having high impurity concentration, and thus it is possible to realize a low ON resistance.

As a method for forming the SJ structure, for example, there is a method of forming a trench in an n type semiconductor layer, burying a p type semiconductor in the trench, and providing a p type semiconductor layer. However, in this method, a hollow portion (empty hole, void) is easily formed inside a p type semiconductor layer.

An example of related art includes International Publication No. 2012-144271.

DESCRIPTION OF THE DRAWINGS

FIGS. 1A and 1B are schematic sectional views of a semiconductor device according to a first embodiment.

FIG. 2 is a schematic top view illustrating a relationship between a length of a second semiconductor region in a direction parallel to a first direction and a length of a third semiconductor region in a direction parallel to the first direction, in the semiconductor device according to the first embodiment.

FIGS. 3A and 3B are schematic sectional views of the semiconductor device in the process of fabrication, based on a fabrication method of the semiconductor device according to the first embodiment.

FIGS. 4A and 4B are schematic sectional views of the semiconductor device in the process of fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIGS. 5A and 5B are schematic sectional views of the semiconductor device in the process of fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIGS. 6A and 6B are schematic sectional views of the semiconductor device in the process of fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIGS. 7A and 7B are schematic sectional views of the semiconductor device in the process of fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIGS. 8A and 8B are schematic sectional views of a semiconductor device according to a second embodiment.

FIG. 9 is a schematic top view illustrating a relationship between a length of a second semiconductor region in a direction parallel to a first direction and a length of a third semiconductor region in a direction parallel to the first direction, in a semiconductor device according to a third embodiment.

DETAILED DESCRIPTION

[0005]Exemplary embodiments provide a semiconductor device which can stabilize characteristics of a super junction structure.

[0006]In general, according to one embodiment, the semiconductor device includes a first electrode; a second electrode; a first semiconductor region of a first conductive type which is provided between the first electrode and the second electrode; a second semiconductor region which is provided to alternate with the first semiconductor region in a first direction of the first semiconductor region and includes a second conductive type impurity; a first insulating region which is provided inside the second semiconductor region; a third electrode which is provided on the first semiconductor region; and a second insulating region which is provided around the third electrode.

[0008]Embodiments of the invention will be hereinafter descried with reference to the drawings. In the following description, the same symbols or reference numerals will be attached to the same members or the like, and description of the members or the like described once will be appropriately omitted.

[0009]In the specification, an upward direction of the drawing is referred to as “upper”, and a downward direction of the drawing is referred to as “lower”, in order to represent a positional relationship of components or the like. In the specification, concept of “upper” and “lower” is not necessarily the terms representing a relationship between directions of gravity.

First Embodiment

[0010]A semiconductor device according to the present embodiment includes a first electrode; a second electrode; a first semiconductor region of a first conductive type which is provided between the first electrode and the second electrode; a second semiconductor region which is provided to alternate with the first semiconductor region in a first direction of the first semiconductor region and includes a second conductive type impurity; a first insulating region which is provided inside the second semiconductor region; a third electrode which is provided on the first semiconductor region; and a second insulating region which is provided around the third electrode.

[0011]FIGS. 1A and 1B are schematic sectional views of a semiconductor device 100 according to the present embodiment. FIG. 2 is a schematic top view illustrating a relationship between a length of a second semiconductor region in a direction parallel to a first direction and a length of a third semiconductor region in a direction parallel to the first direction, in the semiconductor device according to the first embodiment. A cross-sectional view taken along line IA-IA of FIG. 2 is FIG. 1A. A cross-sectional view taken along line IB-IB of FIG. 2 is FIG. 1B. The semiconductor device 100 according to the present embodiment is a vertical MOSFET of a trench gate type having a super junction structure.

[0012]In FIGS. 1A to 2, a first direction is referred to as an X-axis direction, one direction perpendicular to the X-axis direction is referred to as a Y-axis direction (second direction), and a direction perpendicular to the X-axis direction and the Y-axis direction are referred to as a Z-axis direction. A cross section of IA-IA line of FIG. 2 and a cross section of IB-IB line of FIG. 2 are within a plane perpendicular to the Y-axis direction, that is, a plane parallel to an XZ plane. FIGS. 1A and 1B are sectional views within a plane perpendicular to Y-axis direction of the semiconductor device 100, that is, within a plane parallel to the XZ plane. In addition, in other words, FIG. 2 is a schematic top view in a case in which the semiconductor device 100 is viewed in the Z direction.

[0013]The semiconductor device 100 includes a first electrode (source electrode) 4, a second electrode (drain electrode) 6, a first semiconductor region 8 of a first conductive type, a second semiconductor region 10, a sixth semiconductor region 12 of a second conductive type, a seventh semiconductor region 14, a first insulating region 16, a first empty hole 18, a third electrode (gate electrode) 20, a second insulating region (gate insulating film) 22, an eighth semiconductor region 30 of a second conductive type, a ninth semiconductor region 32 of a first conductive type, a tenth semiconductor region 34 of a second conductive type, a third semiconductor region 40, a fourth semiconductor region 42, a third insulating region 46, a second empty hole 48, a fourth insulating region 50, a barrier metal 52, and an upper surface 70.

[0014]Hereinafter, a case in which a first conductive type is an n type, and a second conductive type is a p type will be described as an example. In addition, impurity concentration of a first conductive type is lowered in the sequence of an n+ type, an n type, and an n- type. In the same manner, impurity concentration of a second conductive type is lowered in the sequence of a p+ type, a p type, and a p- type.

[0015]The first electrode 4 is a source electrode of the semiconductor device 100. The first electrode 4 includes, for example, aluminum (Al).

[0016]The second electrode 6 is a drain electrode of the semiconductor device 100. The second electrode 6 includes, for example, vanadium (V), nickel (Ni), gold (Au), silver (Ag), or tin (Sn).

[0017]The first semiconductor region 8 of an n type is provided between the first electrode 4 and the second electrode 6, and includes the upper surface 70. The first semiconductor region 8 includes silicon (Si) including n type impurity. The n type impurity is, for example, phosphorous (P) or arsenic (As). The first semiconductor region 8 is a portion of an n type having a super junction structure.

[0018]The barrier metal 52 is provided between the first electrode 4 and the first semiconductor region 8. The barrier metal 52 prevents aluminum and silicon from diffusing each other due to direct contact between aluminum (Al) for being used for the source electrode 54 which will be described below, and silicon. The barrier metal 52 includes, for example, titanium nitride (TiN), titanium (Ti), or titanium tungsten (TiW).

[0019]A plurality of second semiconductor regions 10 are provided to alternate with the first semiconductor region 8 in a first direction of the first semiconductor region 8. The second semiconductor region 10 includes p type impurity. The p type impurity is, for example, boron (B). The second semiconductor region 10 is a portion of a p type having the super junction structure.

[0020]The second semiconductor region 10 includes the sixth semiconductor region 12 of a p type, and the seventh semiconductor region 14 provided inside the sixth semiconductor region 12. The sixth semiconductor region 12 of a p type includes, for example, silicon (Si) and p type impurity. The seventh semiconductor region 14 includes, for example, i type (non-doped type) silicon (Si).

[0021]The first insulating region 16 is provided inside the seventh semiconductor region 14 (inside the second semiconductor region 10). The first insulating region 16 includes, for example, a silicon oxide (SiO2). The first insulating region 16 includes the first empty hole 18 provided inside the first insulating region 16.

[0022]In the present embodiment, the seventh semiconductor region 14 including i type (non-doped type) silicon (Si) is provided inside the sixth semiconductor region 12. For this reason, p type impurity concentration of the second semiconductor region 10 decreases from the first semiconductor region 8 toward the first insulating region 16, or a region with higher p type impurity concentration is provided on a side near the first semiconductor region 8 rather than the first insulating region 16.

[0023]The third electrode 20 is provided between the plurality of second semiconductor regions 10 on the first semiconductor region 8. The third electrode 20 is a gate electrode of the semiconductor device 100. The third electrode 20 includes, for example, polycrystalline silicon (Si).

[0024]The second insulating region 22 is provided around the third electrode 20. The second insulating region 22 is a gate insulating film of the semiconductor device 100. The second insulating region 22 includes, for example, a silicon oxide (SiO2).

[0025]The eighth semiconductor region 30 of a p type is provided between the second semiconductor region 10 and the third electrode 20. The eighth semiconductor region 30 of a p type is a channel region (base region) of the semiconductor device 100.

[0026]The ninth semiconductor region 32 of an n type is provided between the second semiconductor region 10 and the third electrode 20, on the eighth semiconductor region 30. The ninth semiconductor region 32 of an n type is a source region of the semiconductor device 100.

[0027]The tenth semiconductor region 34 of a p+ type is provided between the second semiconductor region 10 and the ninth semiconductor region 32, on the eighth semiconductor region 30. The tenth semiconductor region 34 of a p+ type is a channel contact region (base contact region) of the semiconductor device 100.

[0028]The third semiconductor region 40 is provided in a second direction perpendicular to the first direction with respect to the second semiconductor region 10. The third semiconductor region 40 includes the fourth semiconductor region 42 of a p type, the third insulating region 46 provided inside the fourth semiconductor region 42, the fourth insulating region 50 provided inside the third insulating region 46, and the second empty hole 48 provided inside the fourth insulating region 50 (third insulating region 46). A length d2 of the third semiconductor region 40 in a direction parallel to the first direction is greater than a length d1 of the second semiconductor region 10 in a direction parallel to the first direction.

[0029]The third insulating region 46 includes, for example, a silicon oxide (SiO2) formed by a thermal oxide method. The fourth insulating region 50 includes, for example, a silicon oxide (SiO2) formed by a chemical vapor deposition (CVD) method, and is formed from boron phosphorus silicon glass (BPSG).

[0030]The second empty hole 48 is connected to the first empty hole 18 in the second direction. In addition, the fourth semiconductor region 42 may be connected to the sixth semiconductor region 12 in the second direction.

[0031]In the semiconductor device 100 according to the present embodiment, a second semiconductor region is further provided in the first direction of the second semiconductor region, as illustrated in FIG. 2. In addition, a third semiconductor region is further provided in the first direction of the third semiconductor region.

[0032]Next, a fabrication method of the semiconductor device 100 according to the present embodiment will be described.

[0033]In the fabrication method of the semiconductor device 100 according to the present embodiment, a first groove whose length in a direction parallel to the first direction is d1 is formed in the second direction perpendicular to the first direction such that the first groove alternates with the first semiconductor region 8 of an n type in the first direction of the first semiconductor region 8 of an n type, a second groove, which is connected to the first groove and whose length in a direction parallel to the first direction is d2 longer than d1, is formed in the second direction, the sixth semiconductor region of a p type is formed on the first groove, the fourth semiconductor region of a p type is formed on the second groove, a seventh semiconductor region of an i type is formed on the sixth semiconductor region, the first empty hole is formed inside the seventh semiconductor region, the fifth semiconductor region of an i type is formed on the fourth semiconductor region, the third insulating region is formed by oxidizing the fifth semiconductor region, the first insulating region is formed around the first empty hole inside the seventh semiconductor region by oxidizing a part of the seventh semiconductor region, the fourth insulating region is formed inside the third insulating region and the second empty hole provided inside the fourth insulating region is formed, the eighth semiconductor region of a p type is formed on the first semiconductor region, the ninth semiconductor region of an n type is formed on the first semiconductor region, the tenth semiconductor region of a p type is formed on the first semiconductor region, the second insulating region is formed on the first semiconductor region, the third electrode is formed on the first semiconductor region, the barrier metal is formed on the first semiconductor region, the source electrode is formed on the first semiconductor region, and the drain electrode is formed so as to come into contact with a surface, which is opposite to a surface on which the source electrode is provided, of the first semiconductor region.

[0034]First, as illustrated in FIG. 3A, the first groove whose length in a direction parallel to the first direction is d1 is formed in the second direction perpendicular to the first direction, such that the first groove alternates with the first semiconductor region 8 of an n type in the first direction of the first semiconductor region 8 of an n type. Subsequently, as illustrated in FIG. 3B, a second groove 62, which is connected to the first groove 60 and whose length in a direction parallel to the first direction is d2 longer than d1, is formed in the second direction.

[0035]Subsequently, as illustrated in FIG. 4A, the sixth semiconductor region 12 of a p type is formed on the first groove 60 by an epitaxial growth method. In addition, the fourth semiconductor region 42 of a p type is formed on the second groove 62 by, for example, an epitaxial growth method. The sixth semiconductor region 12 and the fourth semiconductor region 42 may be coupled to each other in the second direction.

[0036]Subsequently, as illustrated in FIG. 5A, the seventh semiconductor region 14 of an i type (non-doped type) is formed on the sixth semiconductor region 12. At this time, in a portion which is the first groove 60 illustrated in FIG. 4A, an upper portion of the first groove 60 is closed as illustrated in FIG. 5A, and thereby the first empty hole 18 is formed inside the seventh semiconductor region 14.

[0037]Subsequently, as illustrated in FIG. 5B, a fifth semiconductor region 44 of an i type (non-doped type) is formed on the fourth semiconductor region 42. Since a width of the second groove 62 is longer than that of the first groove 60, an upper portion of the second groove 62 is not closed as in the upper portion of the first groove 60.

[0038]Subsequently, as illustrated in FIGS. 6A and 6B, for example, oxygen gas is supplied inside the second groove 62, and thereby the fifth semiconductor region 44 is oxidized. Accordingly, the third insulating region 46 is formed. In addition, the oxygen gas which is supplied inside the second groove 62 is supplied to the first empty hole 18 from the second groove 62. Hence, a part of the seventh semiconductor region 14 is oxidized, and thus the first insulating region 16 is formed inside the first empty hole 18 of the seventh semiconductor region 14.

[0039]Subsequently, BPSG is introduced into the third insulating region 46 by, for example, a CVD method. Then, the fourth insulating region 50 is formed inside the third insulating region 46 and the second empty hole 48 provided inside the fourth insulating region 50 is formed. Subsequently, BPSG is heated thereby being dissolved, and the fourth insulating region 50 reflows inside the third insulating region 46. Subsequently, the surplus fourth insulating region 50 provided on the first semiconductor region 8 is etched, and removed by chemical mechanical polishing (CMP). These processes are illustrated in FIGS. 7A and 7B.

[0040]Finally, the eighth semiconductor region 30 of a p type, the ninth semiconductor region 32 of an n type, and the tenth semiconductor region 34 of a p type are formed on the first semiconductor region 8 by an ion injection method or the like. Subsequently, the second insulating region 22, the third electrode 20, the barrier metal 52, and the first electrode 4 are formed on the first semiconductor region. Subsequently, the second electrode 6 is formed in a manner in contact with a surface, which is opposite to a surface on which the first electrode 4 is provided, of the first semiconductor region 8. Accordingly, the semiconductor device 100 illustrated in FIGS. 1A and 1B is obtained.

[0041]Subsequently, actions and effects of the semiconductor device 100 according to the present embodiment will be described.

[0042]Since a leakage current can flow through a p type portion (second semiconductor region) with a super junction structure, characteristics of a semiconductor device may be not stabilized. In order to reduce the leakage current, it is considered that an insulator such as an oxide film is provided in a part of the p type portion. However, if an insulator is provided on an upper surface 70 of the first semiconductor region 8, a device such as an FET is hardly formed on the insulator, and thus it is difficult to miniaturize a semiconductor device. If an empty hole is provided in a p type portion in order to increase a fabrication speed, a leakage current can flow through an inner wall of the empty hole, and thus the problem is further manifested.

[0043]In the semiconductor device according to the present embodiment, the first insulating region is provided inside the second semiconductor region. For this reason, it is possible to prevent the leakage current from flowing. In addition, since an insulator is not provided on the upper surface 70 of the first semiconductor region, it is possible to miniaturize the semiconductor device.

[0044]A structure in which the first empty hole is formed inside the first insulating region is provided, and thus it is possible to fabricate the semiconductor device in a high fabrication speed, and to prevent the leakage current from flowing through the inner wall of the first empty hole.

[0045]A structure in which second conductive type impurity concentration of the second semiconductor region decreases from the first semiconductor region toward the first insulating region, or a region with high p type impurity concentration is provided near the first semiconductor region 8 rather than first insulating regions 16a and 16b, is provided. Accordingly, by providing the semiconductor region of an i type (non-doped type), the sixth semiconductor region 12 is prevented from being oxidized, and impurity concentration is easily controlled.

[0046]By providing the third semiconductor region separately from the second semiconductor region, it is possible to form the semiconductor device such as an FET on the second semiconductor region, and to prevent the leakage current from flowing by oxidizing the inner wall of the first empty hole.

[0047]A length of the third semiconductor region in a direction parallel to the first direction is greater than that of the second semiconductor region in a direction parallel to the first direction, and thereby it is possible easily close the upper portion of the second semiconductor region without closing the upper portion of the third semiconductor region. As a result, oxygen gas or the like is introduced to the second semiconductor region from the upper portion of the third semiconductor region, and thereby an inner wall of the first empty hole can be oxidized.

Second Embodiment

[0048]A semiconductor device 200 according to the present embodiment is different from the semiconductor device 100 according to the first embodiment in that the semiconductor device 200 includes a vertical MOSFET of a planar gate type with a super junction structure. Here, the same portions as in the first embodiment will not be described.

[0049]FIG. 8 is a schematic sectional view of the semiconductor device 200 according to the present embodiment. In the semiconductor device 200 according to the present embodiment and fabrication method thereof, it is also possible to provide a semiconductor device which can stabilize the characteristics of the super junction structure.

Third Embodiment

[0050]A semiconductor device 300 according to the present embodiment is different from the semiconductor device according to the first embodiment in that a third semiconductor region is provided in the first direction of the second semiconductor region. Here, the same portions as in the first embodiment and the second embodiment will not be described.

[0051]FIG. 9 is a schematic top view illustrating a relationship between a length of the second semiconductor region in a direction parallel to a first direction and a length of a third semiconductor region in a direction parallel to the first direction, in a semiconductor device 300 according to the present embodiment. In this way, by providing the second semiconductor region and the third semiconductor region, more of the second semiconductor region and the third semiconductor region per unit length in the first direction (X-axis direction) can be provided, and thereby it is possible to miniaturize the semiconductor device.

[0052]According to the semiconductor device 300 according to the present embodiment, it is possible to provide a semiconductor device which can be miniaturized and can stabilize characteristics of a super junction structure.

[0053]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first electrode;

a second electrode;

a first semiconductor region of a first conductive type which is provided between the first electrode and the second electrode;

a second semiconductor region which is provided to alternate with the first semiconductor region in a first direction of the first semiconductor region and includes a second conductive type impurity;

a first insulating region which is provided inside the second semiconductor region;

a third electrode which is provided on the first semiconductor region; and

a second insulating region which is provided around the third electrode.

2. The device according to Claim 1, wherein second conductive type impurity concentration of the second semiconductor region decreases from the first semiconductor region toward the first insulating region.

3. The device according to Claim 1 or 2, wherein the first insulating region further includes a first empty hole which is provided inside the first insulating region.

4. The device according to Claim 3, further comprising:

a third semiconductor region which is provided in a second direction perpendicular to the first direction with respect to the second semiconductor region, and includes a fourth semiconductor region of a second conductive type, a third insulating region that is provided inside the fourth semiconductor region, and a second empty hole that is connected to the first empty hole which is provided inside the third insulating region.

5. The device according to Claim 4, wherein a length of the third semiconductor region in a direction parallel to the first direction is greater than a length of the second semiconductor region in a direction parallel to the first direction.

ABSTRACT

According to one embodiment, a semiconductor device includes a first electrode; a second electrode; a first semiconductor region of a first conductive type which is provided between the first electrode and the second electrode; a second semiconductor region which is provided to alternate with the first semiconductor region in a first direction of the first semiconductor region and includes a second conductive type impurity; a first insulating region which is provided inside the second semiconductor region; a third electrode which is provided on the first semiconductor region; and a second insulating region which is provided around the third electrode.